General Remarks / Arguments

Thank you for your thorough review of my application. I realize that the English language sometimes presents difficult choices and constructs that lead to confusing statement. There are numerous instances of new techniques, such as cellular phones, that have replaced or combined or eliminated the structures of previous disclosures. I ask the Examiner if there is currently a Type / Class that better fits the teachings of this application.

Suggestions:

- Class 340, subclass 470 Electronic circuits (Used by Blemel and Asam), or,
- Class 713, subclass 500 Multi-Chip Module instrument controller, or,
- Class 713, subclass 323 Multi-Chip Module instrument controller with power management providing automatic activation/deactivation of processor based on an external signal.

I appreciate the welcoming of material presented in claim 6 with feedback. The explanation (feedback) that the applicant provides is that the current patent application involves analog and digital processing which adapts, diagnoses, prognoses and controls. The software programming is a mixture of conventional compiled and static software, and software is created (instantiated) and/or modified "on-the-fly".

I apologize for the confusion caused by the use of the word "instantiation on-the-fly" which according to dictionary definitions relates to creating instances.

It would be understood by a person familiar with the art of programming, at the time that the current patent application was submitted, that devices relying on preprogrammed instructions were becoming arcane and could be instantiated 'on-the-fly" through automatic code generation (autocoding) and string substitution using "core engines" such as GWBasic™ and JAVA™. The current patent employs this feature of instantiation with automatic code generation and string substitution to advantage. Autocoding was accomplished and published by Christopher Robins, et. al of Management Communications and Controls, Inc. (MCCI) of Arlington Virginia. The website address of MCCI is www.mcci-arl-va.com. Autocoding of software for processors was the subject of the widely published Defense Advanced Research Projects Agency's RASSP (Rapid-prototyping of Application Specific Signal Processors) project managed by Lockheed Martin Advanced Technology Laboratory starting in 1993. The applicant participated in the RASSP project as a scientist and employee of Management Sciences, Inc.

Regarding on-the-fly instantiation of devices, algorithms, applications and processes

In the text of the patent application, in the sections labeled "BACKGROUND – DESCRIPTION OF THE PRIOR ART", "SUMMARY" and other sections, the current patent application teaches creating "on-the-fly" connections, calculus, algorithms and software.

Instantiation lies at the heart of inventions. Static instantiation is common, using permanent connections of devices. For electronic devices instantiation "on-the-fly" is enabled at least by switching with semiconductor technology. For example, the current inventor in Blemel and Asam (U.S. Patent No. 3,566,394) used semi-conductor logic to create analog transforms. There are numerous patents that are based on static interconnection of semiconductors with resistive and capacitive elements, e.g. comparators, summing or differential amplifiers. Blemel and Asam used static gate connectivity to make and manipulate analog trigonometric functions (sine, cosine, arctangent) using binary constructs created by semiconductor gates.

The current invention involves the use of a device such as a Complex Programmable Logic Device (CPLD) or a Field Programmable Gate Array (FPGA) for automated interconnection of semiconductors such as transistors and diode matrices, which are often referred by persons practiced in the art as "gates" because of their switching property, into electronic devices. The power of devices like the FPGA and CPLD make possible routing of connections and devices so that analog and digital devices are created "on-the-fly." In a similar manner the semiconductor material can be constructed into microcomputer circuits (e.g. shift registers, memory, comparators) the processes are a Turing Complete Boolean calculus of bitwise transforms and processes described by computer software algorithms.

Instantiation "on-the-fly" architectures

The current invention teaches a means wherein said process elements operate in parallel or serial manner in plurality of computing architectures instantiated "on-the-fly." The capability to create process elements on-the-fly is in claim 6 amended.

Instantiation "on-the-fly" for adaptive parallel multi-processing

The current patent application, in the section labeled "SUMMARY", teaches: "The present invention is a high precision micro-electronic system that provides the means for real time adaptive parallel multi-processing to monitor and control a plurality of distributed processes without the need for dedicated microprocessors."

Using instantiation on-the-fly for adaptive reconfigurable parallel multi-processing

The current patent application, in the section labeled "SUMMARY", the current patent teaches: "More particularly it relates to an electronic circuit that is a field reconfigurable computing apparatus incorporating a field programmable gate array capable of hosting simultaneously a plurality of parallel computing processes for the purpose of controlling a plurality of distributed or collocated processes ".

Instantiation "on-the-fly" for remotely controlled software programming

The current patent application, in the section labeled "REDUCTION TO PRACTICE" teaches "on-the-fly" programming during operation, e.g. by use of a JTAG programming port.

Unclocked asynchronous multi-threaded operation

The current patent in [0005] states:

> *"The present invention relates to the field of process and machine diagnostics and control, and more specifically to a remotely programmable electronic component constructed of various commodity microcircuits that provide a means for a field programmable distributed control system employing* ***unclocked asynchronous multi-threaded*** *process control that exploits the tight coupling of components from non-similar processes and non-volatile storage for numerous monitoring/controlling applications under conventional and exacting conditions requiring high speed operations."*

Means for Diagnostic and Prognostics

A differentiating innovation of the current patent involves instantiation of calculus and algorithms for diagnostics, prognostics, and control based on processing of weighted parameters.

Operation, unclocked, at the raw speed of the flow of electricity and light

In the case of coupling to analog devices the instantiation is based on electrical processing means such as integrals, differentials, summations of current, voltage using electrical transforms which are performed at the speed of electricity which is the speed of light. This transformation is different from those embodied in software programs which operate at clock speed.

Removal of the need for a dedicated microprocessor

The section labeled "SUMMARY", teaches: "The present invention is a high precision micro-electronic system that provides the means for real time adaptive parallel multi-processing to monitor and control a plurality of distributed processes without the need for dedicated microprocessors." The removal of the need for a dedicated processor found in prior art is differentiating feature of the current patent.

Analog processing and digitized processing in the same device

The current patent application, in the section labeled "REDUCTION TO PRACTICE", teaches that a key discriminating feature of the current device is that the operation goes beyond the prior art by teaching both analog processing and digitized processing in the same device. The text of the current patent states "to achieve high-speed signal processing and digitizing of analog feedback signals to accomplish operating a 100 frames per second." Note: At the time of reduction to practice, prior art, because of clocked processing had been limited to accomplishing one frame per hour. High-speed real time analog signal processing, unlimited by the speed of digitizing of analog signals, was key to realizing this hundred-fold improvement.

Responses to Examiner's Objections

The following paragraphs contain responses to the Examiner's objections in the current Office Action.

A. One basis for the amendments in this response is the words of the Examiner in the Office Action:

"14 As to claim 6, claim 6 is dependent from claim 1 because it has the dependent feature from claim 1. Applicant's feedback regarding this dependency of the claim 6 is welcome in the next response."

Claim 6 was formed as an independent claim not intended to be dependent on claim 1, as shown by the late reference to claim 1.

Remedy found in this response:

a) In claim 6 I have removed the sentence referencing claim 1 making claim 6 an independent claim.
b) I have amended other claims dependent on claim 1 to be dependent on claim 6.

B. The present invention is a control system that operates not by relying only on pre-programming of software and connections but by using the innovation of instantiation of devices, calculus, logic, algorithms and software "on-the-fly" with subsequent release/deconstruction when no longer needed.

1) See BACKGROUND – DESCRIPTION OF PRIOR ART " The FPGA operates either independently or under control of the CPU performing calculus and algorithms."

Staiger, Wynn, and Jennings each teach operating with pre-programmed software stored in memory.

2) *Also see Background – Description of the Prior Art (Col x, lines 1 to 8??) Staiger, Wynn, and Jennings all teach operating with pre-programmed software stored in memory.*
"The primary object of the present invention is to leverage the availability of a large scale FPGA to replace the pre-programmed functionality of the current art microcontroller with freely and remotely programmable architectures of similar functionality and invent the means for implementing an innovative control system based upon such FPGA based technology."

C. The present invention is a control system that operates with combinations of digital, optical and analog processing. See Background – Description of the Prior Art

"Another object of the present invention is to provide a mechanism for overcoming the limitations of prior art by providing a small footprint means for very high speed digitizing and parallel processing, a capability needed to interface and keep pace with purely analog or optical computing architectures that operate at the speed of the electricity or light unlike dedicated digital processor architectures of the current art."

"Another object is to take advantage of the fact that myriad electronic devices can be constructed and deconstructed 'on-the-fly' with gates of portions of the gate arrays. Such devices include tightly coupled adaptive parallel processors and electronic hardware circuits."

Instantiation of devices and connections

The current patent application teaches that the restriction of static coupling and static configuration is unnecessary. The current patent application replaces static interconnection by a capability of interfacing to another FPIC or other processor, made possible by dynamic instantiation "on-the-fly" of the interconnections (a.k.a. coupling). To a person practiced in the art instantiation of the computing architecture is markedly different from selectively changing software.

Unclocked Operation

In the case of coupling to analog devices this instantiation is based on electrical means such as current, voltage, or other electrical transforms which are performed at the speed of electricity which is the speed of light. To a person practiced in the art these transforms are intuitively different from those embodied in software programs which operate at clock speed.

Teaching of Prior Art Referenced by the Examiner

Jennings and Earle (6,449,273) teach a channel communications hub with static interconnections to direct digital signals. For example, Jennings and Earle teach: Multi-port processor 400 can operate as a multi-port processor 320 in FIG. 3. Multi-port processor 400 controls and manages communication through multiple packet-based protocol channels 310.

Jennings and Earle teach a multi-port packet processor and in the Abstract states: "A multi-port packet processor of an integrated circuit provides an efficient means to interface multiple high-speed packet-based communication channels." Further, "this invention relates generally to a computer network". Jennings and Earle teach a digital device. Jennings and Earle, even in light of Wynn and DO NOT teach analog processing in combination with digital processing with both "analog and digital" inputs and both "analog and digital" outputs for controlling processes.

Distributed parallelized hybrid processing (analog and digital)

Jennings and Earle (6,449,273), Staiger (6,292,718), and Wynn et al. (6,275,499) teach a digital processing device. The current patent is not solely a digital device. The current patent teaches a hybrid controller with adaptive flow, a controller with a combination of parallel analog and digital processing. In particular, analog signal processing operations are NOT taught by Jenning's and Earle.

Instantiation "on-the-fly" of parallel computing

The present invention teaches parallelism of asynchronous, non-similar, non-predetermined, processes instantiated "on-the-fly". By having these interconnections and parallel processes instantiated "on-the-fly" the current patent improves on Staiger (6,292,718) which in Staiger's claim 14 teaches "an electronic control system for controlling a processing system, comprising: a plurality of control functions each of a predetermined function and each of which is able to communicate with remaining ones of said control elements, wherein said control elements are arranged in a tetrahedron geometry."

Unclocked, asynchronous operation.

Prior art, taught by Jennings and Earle (6,449,273), Staiger (6,292,718), and Wynn et al. (6,275,499) teach dedicated microprocessors. The current patent teaches elimination of the need for a dedicated clock controlled processor. Further, this ability to work in real time asynchronously is a key and differentiating feature of the current patent over the prior art. In particular, by having these functions operating in real time in an unclocked and asynchronous manner, the current patent improves on Jennings and Earle's Patent No. 6,449,273 which teaches a clocked processor to provide protocol operation.

By having these functions operating in real time in an unclocked and asynchronous manner, the current patent improves on Staiger's patent (6,292,718) which teaches a clock controlled architecture (e.g. PIC or Power PC) with real time operating system (RTOS).

By operating in real time, in an unclocked and asynchronous manner, the current patent overcomes Wynn et al. (6,275,499) which teaches a plurality of dedicated clock controlled processors for the fault tolerant electronic control system.

By operating in real time, in an unclocked and asynchronous manner, the current patent overcomes Staiger's patent (6,292,718) which teaches a clock controlled architecture of multiple processors, that interfaces telecommunications media to a switching matrix as well as, in adaptation, for higher level controller applications.

By operating in real time, in an unclocked and asynchronous manner, the current patent overcomes the limitations of a clock controlled processor taught in Lyke's patent (6,148,399), Quist's patent (6,199,018), Rostoker's patents (5,563,928 and 5,678,057) and Newman's patent (6,049,748) that teach a clock controlled microprocessor.

This feature for asynchronous unclocked operation overcomes the limitations of Jennings and Earle's Patent No. 6,449,273 that teaches a dedicated clock controlled processor to provide protocol operation. Requires a dedicated clock controlled processor to provide control of a processing system.

Specific Response to Examiner's Objections about Informalities

Examiner's item 2: Claim 6 is objected to because of the insufficient antecedent basis for "the monitoring device" (line 4). It is believed that the monitoring device was meant to be the monitoring devices in line 2 of the preamble.

Action taken in this response: Claim 2 was amended to provide sufficient antecedent basis.

Examiner's item 3: Claim 1 recites the limitation of "the architecture" in line 16 due but with insufficient antecedent basis for the limitation.

Action taken in this response: Claim 1 is now canceled. Therefore, the applicant believes the comment is moot.

Examiner's item 4: Claim 8 recites the limitation "the system support applications" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Action taken in this response: Claim 8 was amended to provide the antecedent basis as suggested by the Examiner.

Examiner's item 5: Claim 14 recites the limitation "said FPIC" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Action taken in this response: Claim 14 is canceled. Thus, the applicant believes this rejection to claim 14 is moot.

Responses to Specific Obviousness Rejections to Claims

Examiner's item 6 rejecting claims 1-10: Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jennings, III (6,449,273) in view of Wynn et al. (6,275,499).

Action taken in this response: Claims 1, 7, 8, and 10 are canceled. Thus, the applicant believes this rejection to claims 1, 7, 8, and 10 are moot. Claims 2, 3, 4, 5, 6, and 9 are now amended.

Claim 3 is now amended to show dependence on claim 6.

The current patent describes a hybrid processor, a device with analog and digital processors. Jennings, III discloses a digital data channel device with digital processing controlled by a processor (see 426 in Fig 4a). The device described by Jennings, III is vastly different from the hybrid (analog and digital) signal processing device taught in the current patent. Wynn (6,275,499) teaches also a digital data processor, vastly different from the hybrid (analog and digital) signal processing device taught in the current patent.

The current patent teaches dynamic instantiation (a.k.a. auto-coding) of new programs not previously stored. Jennings, III (Col.4 (lines 20=25) DOES NOT use or infer the word "instantiated". Wynn (6,275,499) teaches redundant connections but DOES NOT teach reconfiguring of interconnections "on-the-fly" or otherwise.

The current patent teaches dynamic use/reuse of the FPIC components including dynamic use/reuse of subelements of components for instantiation of circuits. Jennings, III DOES NOT teach the instantiation of circuits. Wynn DOES NOT use or infer the instantiation of circuits. The current patent teaches dynamic changing of interconnections. Jennings, III (Col.4 (lines 20-25) DOES NOT teach dynamic creating / changing of interconnections "on-the-fly" or otherwise to interconnect newly created devices. Wynn teaches redundant interconnection to redundant devices but DOES NOT teach dynamic changing of interconnections to interconnect newly instantiated devices.

For clarity: the current patent (in original claim 1, now presented as claim 6) teaches "assume roles needed to create" referring to the process of instantiation of the architectures (connections and software) "on-the-fly." This is a new teaching enabled by the dynamic coupling along with dynamic

creation of circuits in the FPGA that define the use of analog circuit transforms in combination with digital processing using algorithm.

The current patent teaches "which has the capability of interfacing to another FPIC or other processor" expressed inter-alia, referring to the process of instantiation (coupling) of the hybrid computing architectures and dynamic programming for digital processors followed by activation. Further, Blemel's teachings, expressed inter-alia and in diagrams, involve a combination of processing analog and digital inputs, digital processing and both analog and digital outputs for process control.

Claim 6 of Jennings and Earle (6,449,273) teaches the port processors permanently coupled to a respective communication channel to provide packet processing and are implemented in one semiconductor integrated circuit. Said packet processing is explained by Jennings as digital.

Claim 7 of Jennings and Earle (6,449,273) teaches that the multi-port processor is configured to operate on packets at the physical layer.

Claim 9 of Jennings and Earle (6,449,273) teaches static "coupling" of digital elements.

Examiner's item 7 regarding claim 1,3:

Action taken in this response: Claim 1 is canceled. Thus, the applicant believes this rejection to claim 1 is moot. Claim 6 amended.

First Argument: By amendment, the antecedent reference of the current patent Claim 3 to Claim 6 teaches that these specific representations in connections, software and hardware are "instantiated on-the-fly" overcoming the limitation in Jennings and Earle (6,449,273) of pre-programmed software and pre-coupled hardware.

"In col.1, lines 55-64, (see also the bit communications in col.4, lines 48-55) Jenning and Earle (6,449,273) *teach a functional defined in a program definition algorithm (see the control program) stored in memory for the purpose of embodiment of that architecture in a portion of the FPGA (see the memory for storing the program to initialize the processor and the program codes in col. 4, lines 20-41)."*

Second Argument: The current patent in claim 7 teaches: The distributed control system as in claim 6 wherein processing elements assume roles..." which create (instantiate) the architectures "on-the-fly" with a combination of analog and digital roles.

Examiner's item 8: "Jennings, III did not specifically show the PCMIA as claimed. However, Wynn disclosed a PCMIA (see fig. 19 [PCMIA], col.15, lines 38-47). It would have been obvious to one of ordinary skill in the art to use Wynn in Jennings, III for including PCMIA as claimed because the use of Wynn could provide Jennings, III the interface capability to adapt to additional system expansion, such as the PCMIA bus, and therefore, increasing the system structure of the processing element in Jennings, and it could be achieved by predefining the R/W ports of the PCMIA of Wynn into the configuration file of Jennings, III so that the connection of PCMIA of Wynn could be recognized by Jennings, III in order to achieve the enhanced system structure, and for the above reason, provided a motivation. Jennings, III is used as primary reference because it showed clearly a plurality of processing elements in a field programmable circuit."

Action taken in this response: Claim 1 is canceled. Thus, the applicant believes this rejection to claim 1 is moot.

Examiner's item 9 rejecting claim 1:

Action taken in this response: Claim 1 is canceled. Thus, the applicant believes this rejection to claim 1 is moot.

Examiner's item 10 is not stated.

Examiner's item 11: "As to claim 2, Jennings, III also included a common access point (see fig.3,[300])"

Action taken in this response: Claim 2, formerly dependent on claim 1, is amended as dependent on claim 6.

Arguments regarding Examiner's item 11: By antecedent reference of claim 2 to claim 1, the current patent teaches that: The common access point can be instantiated (coupled) "on-the-fly"

whereas Jennings and Earle *(6,449,273)* teach a permanent coupling etched into the one semiconductor integrated circuit (see fig 3 [300]).

Examiner's item 12: "As to claim 4, see the micro controller, programmable logic devices, finite state machine in col.4, lines 20-41, see also col.5, lines 1-12)."

Action taken in this response: Clam 4 is now amended to show dependence on claim 6.

Arguments regarding Examiner's item 12: The current patent teaches that the processing elements are calculus and algorithms. To differentiate from preprogrammed software, in the current patent calculus expressions and algorithms are represented as text which are subject to alteration during processing e.g. by software algorithms. The current patent teaches that the processing elements are digital and analog circuits formed in the FPGA or as interconnected circuits, this in addition to analog to digital (A/D) conversion. Jennings and Earle (6,449,273) DOES NOT teach analog processing other than analog to digital conversion.

Examiner's item 13 regarding claim 5: As to claim 5, col.2, lines 12 (asynchronous, ATM), col.4 lines 14-19 (interrupt and clock timer for synchronous, see also the communication control and status through the separate communication mechanisms for col.1, lines 11-26, col.6, lines 5-26 for the serial bus and concurrent data transfer the asynchronous and synchronous in serial and parallel fashion.

Action taken in this response: Claim 5 (formerly dependent on claim 1 is currently amended dependent on claim 6).

Arguments regarding Examiner's item 13: Jennings and Earle *(6,449,273)* teach a STATIC architecture that with the exception of analog to digital (A/D) converters, built of digital circuits of one semiconductor integrated circuit. The current patent in claim 5, described inter-alia in the patent application is performed by architectures that are instantiated on-the-fly with circuits that are analog and digital in addition to A/D converters and D/A converter circuits.

Examiner's item 14: "As to claim 6, claim 6 is dependent from claim 1 because it has the dependent feature from claim 1 (see claim 6, lines 16-17). Applicant's feedback regarding the dependency of the claim 6 is welcome in the next response."

Action taken in this response (providing feedback requested (welcomed) by the Examiner):

Claim 6 is now amended to be independent by removing the reference to claim 1.

Arguments regarding Examiner's item 14: As stated by the Examiner, Jennings does not reference weighing parameters and diagnosing. A person practiced in the art would NOT translate the ability of Jennings III and Earle *(6,449,273)* to use the D/A converter for laser signal conversions as teaching a prior art for weighing parameters and diagnosing.

Jennings and Earle (6,449,273) teaches an Analog to Digital converter (A/D) for digitizing of sensor signals for subsequent digital processing. Jennings and Earle DO NOT teach the combined analog processing of signals from sensors as taught by the current patent. The current patent adds the ability to process the certain analog signals directly, without digitizing, as well as the ability to process certain digital formatted data from sensors. Further, Jennings and Earle (6,449,273) DO NOT teach a centralized data processor coupled to a plurality of local devices that provide the means for monitoring, diagnosing, prognosing and controlling;

Examiner's item 15 and 16: "15. As to claim 7, Jennings, III also included at least:

a) first control for specific functionality of system support (see the support circuit 436);
2) second process control covered all applications related to real time networks (see the real time actions in col.4, lines 46-55),
3) third process included human interface applications (see the I/O analog conversions in col.4, lines 46-55);
4) LAN and WAN (see LAN and WAN for the background in col.1, lines 11-26."

"16. As to the wireless, Wynn also taught wireless (see col.4, lines 40-47)."

Action take in this response: The current patent claim 7 is canceled. Claim 19 is a reworded claim 7. Use of a new claim was because of the extensive deletion required in removing the references to LAN and WAN and wireless and words for adding a fifth process that performs instantiation "on-the-fly" (as found inter alia).

Examiner's item 17: "As to claim 8, Wynn also included at least a fault handling (see col.31, lines 34-47). No specific format of the power management, wake-up, vitality control has been reflected into the claim, therefore it is assumed they are of general type of power management, such as power on, and off

(both teachings in Jennings, III and Wynn), general save mode (not explicitly shown), and the analog signals for the A/D conversions (see Jennings, III, col 4, lines 46-55)."

Arguments regarding Examiner's item 17: As amended, claim 8 power management, wake-up and sleep control, and system vitality monitor are decidedly different from power on and power off taught by Jennings and Earle *(6,449,273)*. The current patent teaches "instantiation" of elements "on-the-fly" during power on, including accumulation of sufficient electrical energy, and selective shutdown during power off to conserve energy.

Further, Wynn et al. (6,275,499) teaches internal fault coverage (read as detection and, in some cases, switchover using redundant circuits) and Wynn teaches use of redundancy but states that loss of both units results in failure. Wynn DOES NOT teach control system fault handling. Wynn specifically teaches that the delivery unit DOES NOT discriminate (internal/external) faults for errors e.g. those detected for the (VT1.5) signals terminated at DS1MX7 308.

Examiner's item 18: "As to claim 9, Jennings also included electro-optic (see the laser in col.4, lines 46-57). As to the electro-mechanic and electro-hydraulic, no specific format or the type of the electromechanically and hydraulic systems has been reflected into the claim, therefore it is assumed any system element which was capable of using the relevant functionalities, such as Jennings III taught a laser converter must connected from laser gun, or the like, therefore it must have been involved with some mechanical and hydraulic mechanisms, although Jennings, III did not explicitly show the mechanical and hydraulic systems, one of ordinary skill in the art should be able to recognize the need of using a mechanical and hydraulic mechanism in general sense to support the laser beams or the laser signals."

Arguments regarding Examiner's item 18: Jennings and Earle *(6,449,273)* teach the term "analog converter" for a device to generate signal states [0,1]. To one practiced in this art, the term "signal state" does not require converting the digital information to analog and thus DOES NOT carry the same meaning as Digital to Analog Converter, which is a device used to create waveforms step-wise proportional to the digital value for driving motors of electro-mechanical systems, electro-hydraulic systems and other devices for stress management and other control functions.

It would be evident to anyone practiced in the art that NOT all signal states are specific analog voltages (e.g. 0 Volts is "0" and 5 volts is "1". Jennings and Earle's description in Col.4, lines 46-57 states: "Support circuits 426 can provide analog conversion for different physical signal states for

communicating (digital) bits on the coupled communication channel. For example, this analog conversion can transform logic signal (e.g. for zero and one) to drive a laser which requires a different signaling convention."

To one practiced in the art of laser communication a laser signaling convention is a digital (binary) protocol". The current patent teaches electromechanical and hydraulic thus DOES NOT have Jenning's restriction.

Examiner's item 19 rejecting claim 10

Action take in this response: Claim 10 is canceled. Therefore the applicant believes the rejection of claim 10 is moot.

Examiner's item 20 rejecting claim 11

Action take in this response: Claim 11 is canceled. Therefore the applicant believes the rejection of claim 11 is moot.

Examiner's item 21 rejecting claim 12

Action take in this response: Claim 12 is canceled. Therefore the applicant believes the rejection of claim 12 is moot.

Examiner's item 22 rejecting claim 13

Action take in this response: Claim 13 is canceled. Therefore the applicant believes the rejection of claim 13 is moot.

Examiner's item 23 rejecting claim 14

Action take in this response: Claim 14 is canceled. Therefore the applicant believes the rejection of claim 14 is moot.

Examiner's item 24 rejecting claim 15

Action take in this response: Claim 15 is canceled. Therefore the applicant believes the rejection of claim 15 is moot.

Examiner's item 25 rejecting claim 16

Action take in this response: Claim 16 is canceled. Therefore the applicant believes the rejection of claim 16 is moot.

Examiner's item 26 rejecting claim 17

Action take in this response: Claim 17 is canceled. Therefore the applicant believes the rejection of claim 17 is moot.

Examiner's item 27 rejecting claim 18

Action take in this response: Claim 18 is canceled. Therefore the applicant believes the rejection of claim 18 is moot.

Examiner's item 28: "The prior art made of record and not relied upon is considered pertinent to the applicant's disclosure.

a) Bell et al. (5,892,767) is cited for the specific teaching of the combination of a plurality of the programmable logic processing elements with external connections. (see col.6, lines 66-67, col.7, lines 1-10).

Arguments regarding Examiner's item 28: Bell's patent DOES NOT teach using "instantiated on-the-fly" connections to a plurality of the programmable logic processing elements, or instantiated on-the-fly software.

Allowable Subject Matter

In item 14 on page 6 of the Office Action, the Examiner indicated that applicant's feedback regarding the dependency of claim 6 is welcome in the next response. Applicant has provided feedback and has made

claim 6 the principle independent claim. Accordingly, Applicant believes amended independent claim 6 to be allowable and respectfully requests removal of this objection.

New Claims

Applicant has added new claim 19.

Claim 19 is an amendment of claim 7. Use of a new claim was because of the extensive deletion required in removing the references to LAN and WAN and wireless and words for adding a fifth process that performs instantiation "on-the-fly" (as found inter alia).

The applicant believes no new material has been added.

Conclusion

This application should now be in condition for a favorable action. Applicant respectfully requests entry of the Amendment and an early allowance of all claims herein. If for any reason the Examiner finds the application other than in allowance, the Examiner is requested to call the undersigned inventor at the below-listed telephone number to discuss steps necessary for placing the application in condition for allowance. If there are any fees due in connection with the filing of this Amendment, they will be paid by funds transfer according to the fee schedule of the U.S. Patent and Trademark Office.

Respectfully Submitted,

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